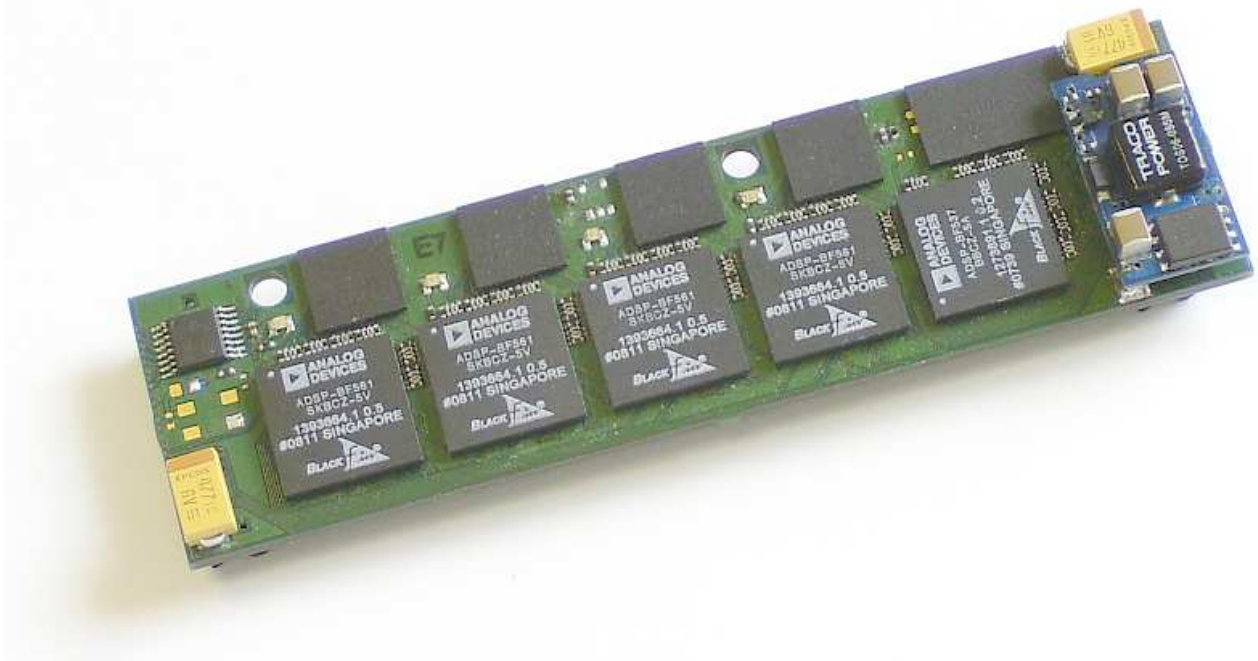


# BF561MULTIcore

Hardware User Manual



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### Important notice:

The information provided in this manual is believed to be accurate and up-to-date at the time of print (2009-12-22). However, no responsibility is assumed for damages arising from the use of the hardware described herein, nor for the suitability for a certain purpose.

The user is responsible to obey all applicable regulations regarding electro-magnetic emissions and susceptibility.

# 1 Introduction

BF561MULTICore is a miniature-size multi-DSP system based on Analog Devices Blackfin processors. It contains one BF537 (500MHz) and four BF561 (600 MHz) dual-core DSPs. The BF537 DSP is capable of running uClinux. It can communicate via Ethernet if an external PHY is added to the system.

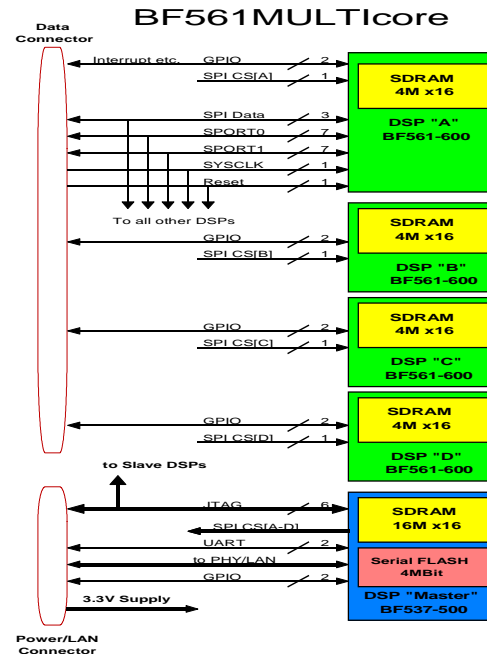
The combination of 9 DSP cores yields a simply-structured high-performance DSP controller board for all sorts of embedded applications, e.g. multi-channel speech transcoders.

With a size of 25.4 x 94.4 mm, the board will fit every embedded platform. High density connectors provide access to the DSP's Ethernet MII signals as well as to the cascaded serial ports of all five DSPs and their JTAG interfaces.

The BF537 can load applications via TFTP and boot the four BF561 DSPs. Alternatively, the DSPs can be booted via SPI directly via the connectors.

## 2 Functional Specification

The following functional diagram of the BF561MULTICore illustrates the signals available on the two connectors and the internal connections on the module.



<b>DSPA-D</b>	BF561 dual-core Blackfin processor with external 4M x 16 RAM
<b>Master DSP (E)</b>	BF537 single core Blackfin processor with external 16M x 16 RAM
<b>Reset-Input</b>	External RESET signal to reset all DSPs
<b>SYSCLK</b>	DSP System Clock: Either on-board oscillator or can be applied externally (LVDS or TTL)
<b>Serial Flash</b>	4 Mbit serial flash available via SPI-interface on Master DSP for booting and storing data.
<b>JTAG</b>	Separate JTAG-connection for DSP. All DSPs are linked in a JTAG chain
<b>SPORT0, 1</b>	All DSPs have their SPORTs linked together for data transfer. Clocks can be applied externally (LVDS or TTL) or one of the DSPs can be master.
<b>UART</b>	UART0 of the master DSP is available at the connector.
<b>SPI</b>	DSPs A-D can either be booted externally, or by the master DSP. The master DSP can also be booted via its local serial Flash ROM.

## 3 Hardware Components

The components of the BF561MULTICore are described in detail in this chapter.

### 3.1 DSPs

The BF561MULTICore-Module is populated with a DSP Blackfin ADSP-BF537BBCZ-5A, running at a maximum speed of 500 Mhz and four DSPs Blackfin ADSP-BF561BSKBCZ-6A, running at a maximum speed of 600MHz.

The on-board oscillator has a clock frequency of 25 MHz. Alternatively, an external clock can be applied with only minor modifications necessary.

For details about the processor's features, refer to [1]. Details about programming the DSP are described in [2].

### 3.2 BF537 SDRAM

The BF537 master DSP has a Micron MT48LC16M16A2 (16Mx16) SDRAM connected to its EBIU. The maximum SDRAM bus frequency of the BF537 is 125 MHz with the master DSP is running at full speed.

The SDRAM is organized in four banks, selected by DSP address lines A18 and A19. It uses 13 row address lines and nine column address lines.

The SDRAM is visible from address 0x0000 0000 up to address 0x01FF FFFF. The following values can be used to setup the SDRAM-controller of the DSP. The refresh rate is dependent on the system clock set with the PLL settings of the DSP. The values indicated are used for a system clock of 125 MHz.

Register	Value
SDGCTL	0x0091998D
SDBCTL	0x00000013
SDRRC	0x000003CD

More details about the Blackfin's SDRAM controller can be found in [1] and [2].

### 3.3 BF561 SDRAM

The BF561s each have a Micron MT48LC4M16A2 (4Mx16) SDRAM connected to their EBIU ports. The SDRAM bus frequency will have to be 120 MHz for optimal performance.

From DSP side, the SDRAM is visible from address 0x0000 0000 up to address 0x003F FFFF. The following values can be used to setup the SDRAM-controller of the DSP. The refresh rate is dependent on the system clock set with the PLL settings of the DSP. The following values are used for a system clock of 120 MHz.

Register	Value
SDGCTL	0x0091998D
SDBCTL	0x00000001
SDRRC	0x00000397

### 3.4 Serial Flash

A serial SPI flash M25P40 from Numonyx with a capacity of 4 Mbits is connected to the BF537 master DSP via its SPI. The serial flash is used for booting and for storing data. It can be erased sector wise. The lowest sector must be used for booting the DSP.

The DSP will boot from the serial flash, when the boot mode is set to “SPI Master”.

For SPI Master Boot R614 and R617 have to be populated with 0R. R615 and R616 have to be left unpopulated. For SPI Slave Boot R615 and R616 have to be populated with 0R. R614 and R617 have to be left unpopulated.

The flash has to be programmed with a loader file for booting from SPI flash that is generated by ADI VisualDSP++ or by the GNU tools.

For more details about the flash, refer to the data sheet [3].

### 3.5 Ethernet-MAC

The BF561MULTICore module has a standard MII ethernet interface routed to its power/LAN connector. This interface allows an easy connection to any standard Ethernet PHY (such as a Teridian 78Q2123).



## Connector rows A and B

Pin No	Signal	Type	Function	Pin No	Signal	Type	Function
A1	HWAIT	O	SPI HostWait	B1	n.c.	n.c.	No Function
A2	n.c.	n.c.	No Function	B2	GPIO8	I/O	GPIO DSP D
A3	SPI_MOSI	I/O	SPI	B3	GPIO7	I/O	GPIO DSP D
A4	GPIO2	I/O	GPIO DSP A	B4	SPI_CS_D#	I/O	SPI
A5	GPIO1	I/O	GPIO DSP A	B5	GPIO6	I/O	GPIO DSP C
A6	SPI_CS_A#	I/O	SPI	B6	VCC3.3	PWR	PWR
A7	SPI_CS_B#	I/O	SPI	B7	VCC3.3	PWR	PWR
A8	GPIO3	I/O	GPIO DSP B	B8	VCC3.3	PWR	PWR
A9	GPIO4	I/O	GPIO DSP B	B9	GPIO5	I/O	GPIO DSP C
A10	SPI_CS_C#	I/O	SPI	B10	RESET#	I	BF537 Reset
A11	GND	PWR	PWR	B11	GND	PWR	PWR
A12	GND	PWR	PWR	B12	GND	PWR	PWR
A13	GND	PWR	PWR	B13	UART0TX	I/O	DSP E UART
A14	FS0	I/O	DSP SPORT 0	B14	UART0RX	I/O	DSP E UART
A15	FS1	I/O	DSP SPORT 1	B15	GND	PWR	PWR
A16	SPI_SCLK	I/O	SPI	B16	DT0PRI	I/O	DSP SPORT 0
A17	DR1PRI	I/O	DSP SPORT 1	B17	GND	PWR	PWR
A18	DR0PRI	I/O	DSP SPORT 0	B18	SCLK1-	LVDS	DSP SPORT 1
A19	SPI_MISO	I/O	SPI	B19	SCLK1+	LVDS / TTL	DSP SPORT 1
A20	DT1PRI	I/O	DSP SPORT 1	B20	GND	PWR	PWR
A21	DT0SEC	I/O	DSP SPORT 0	B21	DSP_CLK+	LVDS / TTL	DSP CLOCK
A22	DR0SEC	I/O	DSP SPORT 0	B22	DSP_CLK-	LVDS	DSP CLOCK
A23	DR1SEC	I/O	DSP SPORT 1	B23	GND	PWR	PWR
A24	DT1SEC	I/O	DSP SPORT 1	B24	SCLK0-	LVDS	DSP SPORT 0
A25	SPI_CS_E#	I/O	SPI	B25	SCLK0+	LVDS / TTL	DSP SPORT 0

There are several options to provide power to the BF561MULTICore:

3.3VDC for all I/O pins is always provided through pins B6, B7 and B8. Typically, no more than 1000mAmps are required for all I/O pins and SDRAM active.

The core voltage can either be generated on board or, if the DC/DC brick is not populated, by applying 1.25VDC to pins C22, C23, C24 and C25. The load at these pins is totalling approx. 5 Amps.

Normally, 3 .. 5VDC are applied to pins C1, C2, C3, D1, D2 and D3 with the DC/DC brick populated. The DC/DC brick generates the core voltage locally. At 3.3VDC, the current drawn on these pins is 2 Amps, typically.

Some of the power supply options are available on request, only.

## Connector rows C and D

Pin No	Signal	Type	Function	Pin No	Signal	Type	Function
C1	VCC3.3-5.0	PWR IN	VCORE	D1	VCC3.3-5.0	PWR IN	VCORE
C2	VCC3.3-5.0	PWR IN	VCORE	D2	VCC3.3-5.0	PWR IN	VCORE
C3	VCC3.3-5.0	PWR IN	VCORE	D3	VCC3.3-5.0	PWR IN	VCORE
C4	GND	PWR	PWR	D4	ETXEN	O	ETHERNET
C5	GND	PWR	PWR	D5	ETXD3	O	ETHERNET
C6	GND	PWR	PWR	D6	ETXD2	O	ETHERNET
C7	GND	PWR	PWR	D7	ETXD1	O	ETHERNET
C8	VADJ	PWR	PWR (leave unconnected)	D8	ETXD0	O	ETHERNET
C9	GND	PWR	PWR	D9	ETXCLK	O	ETHERNET
C10	ECRS	I	ETHERNET	D10	EMDIO	I/O	ETHERNET
C11	ERXD2	I	ETHERNET	D11	EMDC	O	ETHERNET
C12	ERXER	I	ETHERNET	D12	ERXDV	I	ETHERNET
C13	ERXD1	I	ETHERNET	D13	ECOL	I	ETHERNET
C14	ERXCLK	I	ETHERNET	D14	ERXD3	I	ETHERNET
C15	ERXD0	I	ETHERNET	D15	EPHYINT#	I	ETHERNET
C16	GND	PWR	PWR	D16	GND	PWR	PWR
C17	TDI	I	DSP JTAG	D17	EMU#	O	DSP JTAG
C18	TCK	I	DSP JTAG	D18	TRST#	I	DSP JTAG
C19	TMS	I	DSP JTAG	D19	TDO	O	DSP JTAG
C20	GND	PWR	PWR	D20	GND	PWR	PWR
C21	GND	PWR	PWR	D21	GND	PWR	PWR
C22	VCC1.25	PWR OUT	PWR (leave unconnected)	D22	GND	PWR	PWR
C23	VCC1.25	PWR OUT	PWR (leave unconnected)	D23	GND	PWR	PWR
C24	VCC1.25	PWR OUT	PWR (leave unconnected)	D24	GND	PWR	PWR
C25	VCC1.25	PWR OUT	PWR (leave unconnected)	D25	GND	PWR	PWR



### 4.3 DSP Booting

There are several ways to boot the DSPs on the BF561MULTIcore module.

Each DSP can be booted separately by an external host via SPI using SPI\_MISO, SPI\_MOSI, SPI\_CLK and the dedicated chip selects (SPI\_CS\_A# - SPI\_CS\_E#). For details, refer to [1] and [2].

Another option is to use the serial Flash ROM on the BF561MULTIcore. This Flash ROM is connected to master DSP capable of booting itself via SPI. In order to use this Boot mode, please refer to Chapter 3.4 (Serial Flash). Once the master DSP has been booted, it can boot the other DSPs (DSP A – D). The master DSP must be re-configured to become an SPI Master and to take control of the SPI chip selects (SPI\_CS\_A# - SPI\_CS\_D#).

### 4.4 Reset

The master DSP (BF537) can be reset using an external reset signal. Pin B10 of the connectors is connected to the input of a TPS3825 reset controller. This controller only resets the BF537 only. The other DSPs receive their common reset signal from Port G Pin0 of the master DSP. Note that you have to release the other DSPs from their reset state, by setting BF537 Port G0 high. Port G0 is pulled down by a resistor so as to keep the BF561's in reset while the master DSP is still booting.

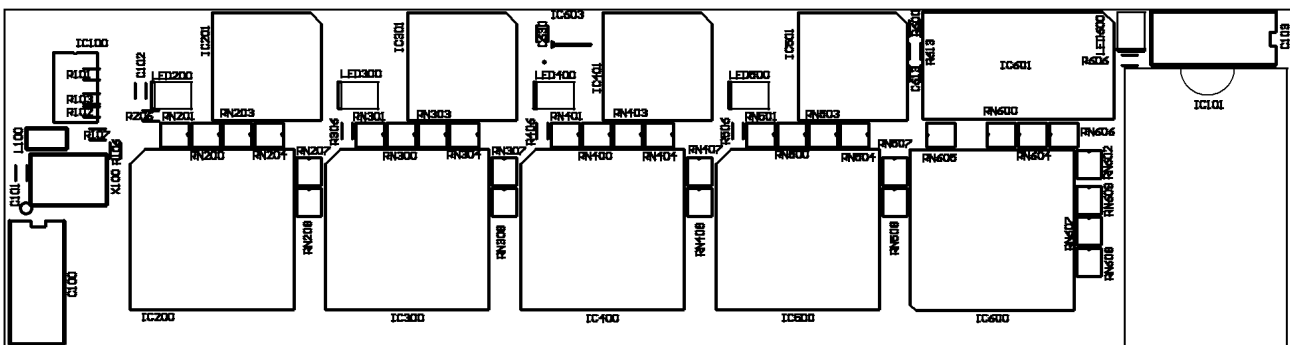
### 4.5 Electrical Characteristics

The board needs 3.3Volts (500mA) on Pins B6 – B8 (+/- 5%). The core voltage can be applied separately to Pins C1 – C3 and D1 – D3. Here a voltage between 3.0 and 5.0 V (3A) is needed.

All DSPs need a core voltage of 1.25V (+/- 5%), which is generated with the voltage generator on the BF561MULTIcore board. It takes its power from pins C1 – C3 and D1 – D3. If desired, the core voltage can be generated externally and be applied to pins C22 – C25. **Note: Remove the voltage converter (IC101) if the core voltage is applied externally.**

The power dissipation depends on the processor load.

### 4.6 Silkscreen



## 5 Bibliography

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<http://www.erni.com/DB/PDF/MicroStac/ERNI-MicroStac-e.pdf>

## 6 Support

Support for this product is available from:

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